



MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

(UGC – AUTONOMOUS INSTITUTION)

MADANAPALLE – 517325 (A.P)

(Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi)

Estd: 1998 Registration form for M. Tech (VLSI & Embedded Systems)– I Year I Semester (R24)

(For 2024 admitted batch)

(All the below details are mandatory and should be filled carefully)

M. Tech

Whether the Candidate is appearing for Regular Examinations Supplementary Examinations

Month & Year of Examination

H.T .No.

Table with 18 columns for Name: (As per S.S.C Certificate)

Table with 18 columns for Father's Name: (As per S.S.C Certificate)

Table with 18 columns for Mother's Name: (As per S.S.C Certificate)

Date of Birth (As per SSC): (DD/MM/YYYY)

Contact No:

Tick [√] the appropriate box

Gender table with Male and Female options

Physically Handicapped (PH) table with Yes and No options

Caste table with SC, ST, BC-A, BC-B, BC-C, BC-D, BC-E, OC options

Course for which registration is required: Tick [√] the appropriate box

Table listing course options with checkboxes for registration

Certified that the above information is CORRECT and filled by me.

Signature of the Candidate



H.T.No.

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Centre:

Madanapalle Institute of Technology & Science

Please affix your latest passport size – colour photograph

1. Name of the Candidate:
2. Father's Name:
3. Month and Year of Examination:
4. Regular /Supplementary:

Tick [] the appropriate box to register for a course

1	24VESP101	CMOS Digital IC Design			24VESP404	Low Power VLSI Design		
2	24VESP102	Microcontrollers and Programmable Digital Signal Processors			4	24VESP405	Nano-materials and Nanotechnology	
3	24VESP403	FPGA Architectures and Applications			4	24VESP406	Network Security and Cryptography	
	24VESP401	Communication Buses and Interfaces				5	24RMP101	Research Methodology and IPR
	24VESP402	Data Acquisition System Design			6	24VESP201	CMOS Digital IC Design Laboratory	
					7	24VESP202	Microcontrollers and Programmable Digital Signal Processors Laboratory	

Signature of the Candidate

Controller of Examinations

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Instructions to Candidates

The candidate has to:

1. Display his/her ID card for verification.
2. The candidate has to confirm himself/herself that he/she does not possess any foreign material, electronic gadgets other than electronic calculator.
3. Candidates should stay in the examination hall at least half-an-hour from the commencement of the examination.
4. Be present in the examination hall 15 minutes before the time of commencement of examination.
No candidate will be allowed after the commencement of the examination.



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Hall Ticket
Original

M. Tech

Estd: 1998

H.T.No.

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1	24VESP101	CMOS Digital IC Design			24VESP404	Low Power VLSI Design	
2	24VESP102	Microcontrollers and Programmable Digital Signal Processors			4	24VESP405	Nano-materials and Nanotechnology
	24VESP403	FPGA Architectures and Applications				24VESP406	Network Security and Cryptography
3	24VESP401	Communication Buses and Interfaces			5	24RMP101	Research Methodology and IPR
	24VESP402	Data Acquisition System Design			6	24VESP201	CMOS Digital IC Design Laboratory
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